

## Materials Science

Special Topic: Two-dimensional Materials and Devices

## Two-dimensional transition metal dichalcogenides for post-silicon electronics

Xiankun Zhang<sup>1,2,#</sup>, Hang Zhao<sup>1,2,#</sup>, Xiaofu Wei<sup>1,2</sup>, Yanzhe Zhang<sup>1,2</sup>, Zheng Zhang<sup>1,2,\*</sup> & Yue Zhang<sup>1,2,\*</sup><sup>1</sup>Academy for Advanced Interdisciplinary Science and Technology, Beijing Advanced Innovation Center for Materials Genome Engineering, University of Science and Technology Beijing, Beijing 100083, China;<sup>2</sup>Beijing Key Laboratory for Advanced Energy Materials and Technologies, School of Materials Science and Engineering, University of Science and Technology Beijing, Beijing 100083, China

#Contributed equally to this work.

\*Corresponding authors (emails: [zhangzheng@ustb.edu.cn](mailto:zhangzheng@ustb.edu.cn) (Zheng Zhang); [yuezhang@ustb.edu.cn](mailto:yuezhang@ustb.edu.cn) (Yue Zhang))

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**Abstract:** Rapid advancements in information technology push the explosive growth in data volume, requiring greater computing-capability logic circuits. However, conventional computing-capability improving technology, which mainly relies on increasing transistor number, encounters a significant challenge due to the weak field-effect characteristics of bulk silicon-based semiconductors. Still, the ultra-thin layered bodies of two-dimensional transition metal dichalcogenides (2D-TMDCs) materials enable excellent field-effect characteristics and multiple gate control ports, facilitating the integration of the functions of multiple transistors into one. Generally, the computing-capability improvement of the transistor cell in logic circuits will greatly alleviate the challenge in transistor numbers. In other words, one can only use a small number, or even just one, 2D-TMDCs-based transistors to conduct the sophisticated logic operations that have to be realized by using many traditional transistors. In this review, from material selection, device structure optimization, and circuit architecture design, we discuss the developments, challenges, and prospects for 2D-TMDCs-based logic circuits.

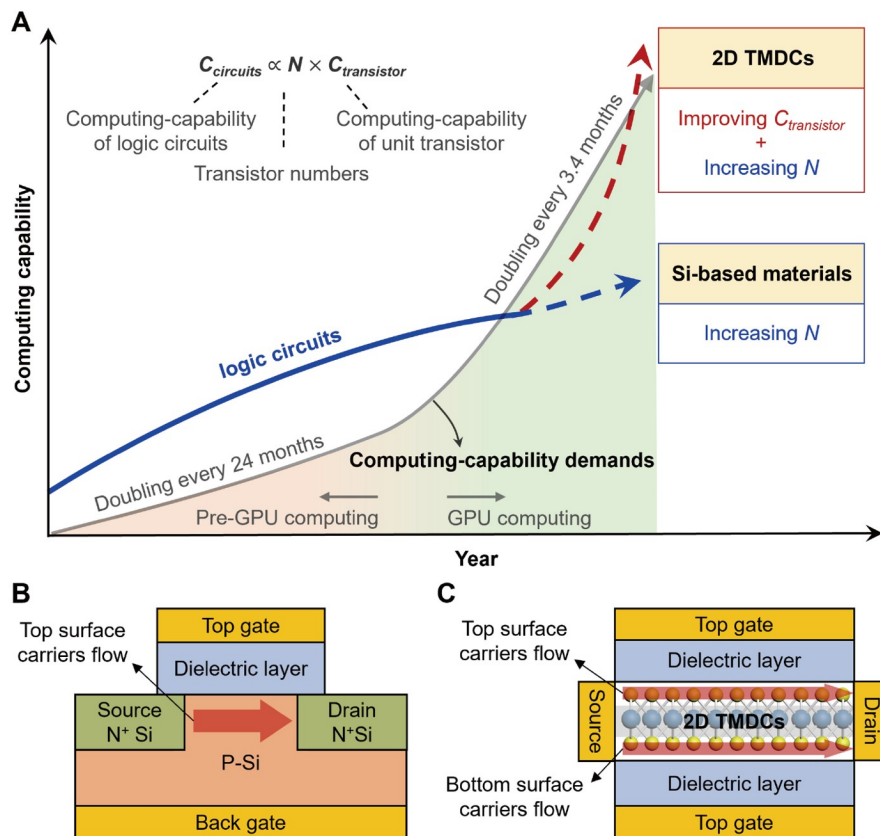
**Keywords:** logic circuits, two-dimensional transition metal dichalcogenides, computing capability, post-silicon electronics, transistor number

### Introduction

As the Internet of Things, artificial intelligence, and cloud computing technologies continue to spread, the data volume has grown explosively. The information volume that needs to be processed per unit of time has increased dramatically resulting in an urgent demand to improve the computing capability of logic circuits [1]. Field-effect transistors (FETs) are the basic building blocks of logic circuits, and their size follows the Dennard effect to keep scaling down, enabling the integration density of transistors in logic circuits to keep increasing [2]. As the number of components integrated into logic circuits doubles every 18 months, the computing capability of the logic circuit doubles [3]. However, when the FET size is shrunk to below 4 nm, the silicon-based channel materials will encounter severe carrier scattering, which leads to a significant

decrease in mobility. Thus, traditional technology relying on reducing transistor sizes to increase circuit integration and thus improve logic circuit performance is facing a significant challenge (Figure 1A) [4].

To immigrate this problem, broadening the function of unit transistors is considered a potential solution for the development of powerful computing-capability (PCC) logic circuits [5]. The core principle is that by designing the PCC transistor based on the original circuit space, more logic functions can be integrated. Compared with conventional architectures, PCC transistor architectures save transistor numbers when satisfying the same computing requirements. However, due to the inherent thickness of silicon-based semiconductors, doping in the source and drain regions is difficult to cover the bottom region, resulting in difficulties for the source and drain to collect carriers in the bottom channel in Figure 1B [6]. The performance modulation of the channel material is only influenced by the top gate, which greatly limits the flexibility of transistor regulation [7]. In addition, the polarity of silicon-based semiconductors is determined by the doping process and is difficult to be modulated by the gate [8]. A single transistor can only be interconnected to achieve a logic function, limiting the application to PCC transistors. Therefore, to meet the high-performance requirements of post-silicon logic circuits, the development of new-principles devices



**Figure 1** The trends in computing-capability of logic circuits and the demands. (A) Trends in increasing demand for computing capability and scaling trends in transistor density. By 2012, computing-capability demand was doubling every 24 months; recently, this has been shortened to approximately every 3.4 months. Si-based logic circuits rely on increasing transistor numbers and thus cannot keep pace with the demand for computing capability. 2D TMDCs-based logic circuits relying on improving the computing capability of the unit transistor will bring powerful computing capacity to meet demand.  $C_{transistor}$  represents the amount of computing capability provided per unit transistor;  $C_{circuits}$  represents the computing capability of logic circuits;  $N$  represents transistor numbers. Reproduced with permission from [1]. Copyright©2022, Springer Nature. Reproduced with permission from [17]. Copyright©2020, Royal Society. (B) Structure diagram of Si-FETs. (C) Structure diagram of the 2D FETs. A single 2D transistor has two surface channels and can be modulated by a vertical double gate.

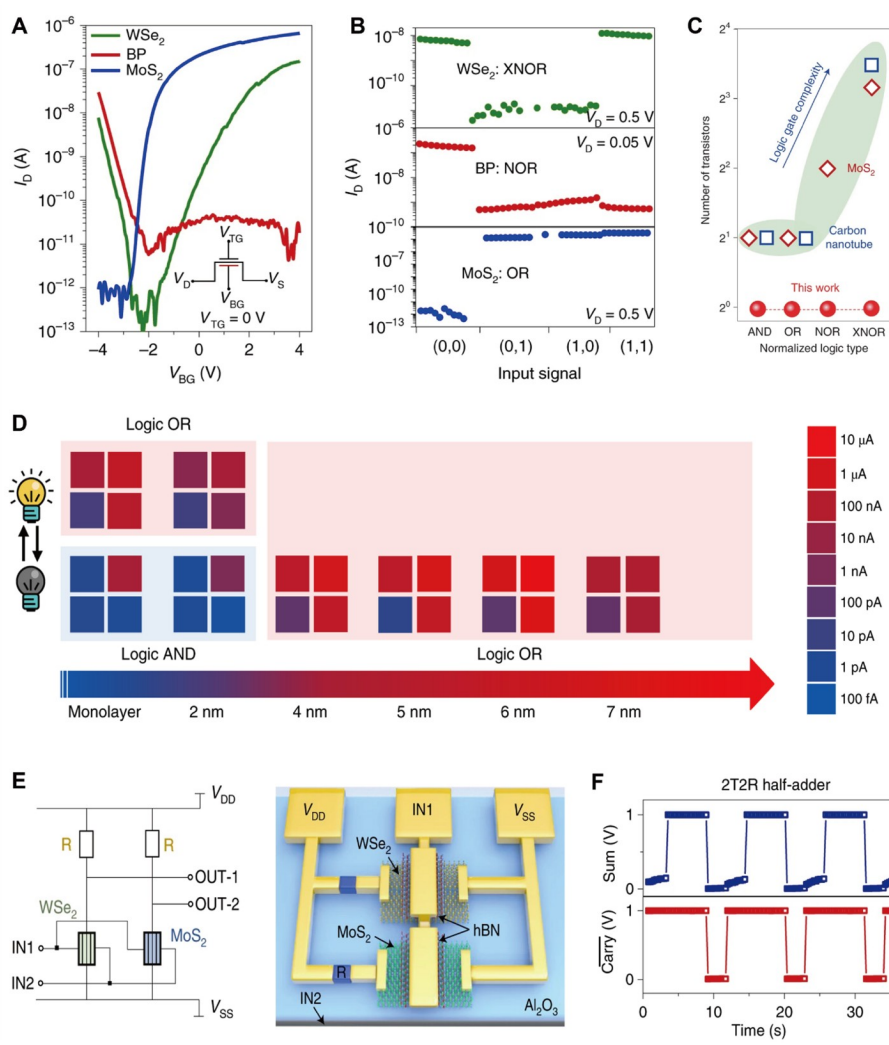
based on new semiconductors is urgently needed.

As an emerging family of semiconductors, ultrathin two-dimensional transition metal dichalcogenides (2D-TMDCs) semiconductors have atomically flat and bonding-free surfaces, which greatly reduce surface scattering effects and thus provide excellent electrical performance even in monolayer cases [9–12]. On the other hand, due to the high electrostatic regulation ability, ultrathin 2D-TMDCs semiconductors have strong immunity to the short channel effect and have been successfully used to construct transistors with the smallest gate length of  $\sim 0.34$  nm [13,14]. More interestingly, a single 2D-TMDCs-based transistor has two surface channels, illustrating the transport characteristics of the transistor can be regulated separately by the top and bottom gates (Figure 1C), which greatly broadens the logic operation function of the transistor [15]. Traditional transistors made of thick bulk semiconductors can only integrate one surface channel. By using multiple gates in concert, only one 2D-TMDCs-based transistor can conduct the sophisticated logic operations that have to be realized by many traditional transistors [16]. In addition to the improvement of computing capability, 2D-TMDCs have obvious advantages in suppressing leakage current, improving transistor integration, and developing flexible devices. Therefore, combined with the advantages of 2D-TMDCs in suppressing leakage current, improving circuit integration, and developing flexible devices, we believe that taking full advantage of 2D-TMDCs will continue to improve the overall performance of post-silicon logic circuits.

This review focuses on the progress, challenges, and future development opportunities of 2D-TMDCs-based logic circuits, and demonstrates an alternative method for fulfilling the growing need for computing capability. We first present the use of the material's intrinsic properties to achieve different logic functions and expand the functionality of a single transistor. Designs for PCC-FET structures and circuit structures are described, which save transistor count when satisfying the same computational requirements. Subsequently, the important challenges from materials to integration applications are also discussed, focusing on 2D-TMDCs-based PCC-FETs for logic circuit development. Finally, new perspectives on the application of 2D-TMDCs-based PCC transistors are proposed.

## **Selection and optimization of 2D-TMDCs material for PCC logic circuits**

2D-TMDCs have a wide range of families and offer a variety of options for device design. Due to the unique layer structure of 2D-TMDCs, their electrons are localized in the surface channels and easily modulated by the gate, which provides new ideas for device structure novelty. Utilizing the advantages of 2D-TMDCs, more logic functions will be offered through circuit design. In Si-based semiconductors, the electrical properties of the material are changed by doping processes. As the dimensions of the devices are downscaled, the inevitable doping and activation processes in the source/drain region can cause problems with random dopant fluctuations [18]. This can lead to significant variations in the threshold voltage and sub-threshold swing of the device, which is detrimental to integration development [19]. The intrinsic polarity of 2D-TMDCs covers p-type, bipolar, and n-type, allowing the design of different electronic devices without additional doping techniques [10,20]. As one of the most widely studied materials for TMDCs,  $\text{WSe}_2$  has bipolar semiconductor properties and is widely used in new logic devices [21]. In Figure 2A, the  $\text{WSe}_2$  transistor exhibits bipolar transport characteristics. In contrast, the  $\text{MoS}_2$  transistor shows typical n-type



**Figure 2** Material engineering for 2D-TMDCs PCC logic devices. (A) Transfer curves of bipolar WSe<sub>2</sub>, p-type BP, and n-type MoS<sub>2</sub> transistors. The top-gate voltage  $V_{TG} = 0$  V, the drain voltage  $V_{DS} = 0.5, 0.05, \text{ and } 0.5$  V, respectively. (B) Bipolar WSe<sub>2</sub>, p-type BP, and n-type MoS<sub>2</sub> FET can implement XNOR, NOR, and OR logic functions, respectively. (C) Comparison of the number of transistors consumed by different materials, with brown diamonds and blue squares representing MoS<sub>2</sub>-based pseudo-NMOS circuits and carbon nanotubes, and red globes representing 2D PCC transistors. (D) Relationship between the thickness of MoS<sub>2</sub> material and the logic function realized by transistors: when the thickness is greater than 4 nm, the logic function is OR, when the MoS<sub>2</sub> thickness is less than 4 nm, the logic function is AND, and using light, the logic function (AND and OR) can be switched. (E) Circuit schematic of a 2T2R-based half adder that utilizes a dual-gate WSe<sub>2</sub> transistor and a MoS<sub>2</sub> transistor interconnected with two fixed-value resistors. (F) The output waveform of the half adder. (A)–(C), (E), (F) Reproduced with permission from [22]. Copyright©2019, Springer Nature. (D) Reproduced with permission from [16]. Copyright©2021, Springer Nature.

transport properties.

Utilizing the different inherent polarities of 2D semiconductors, transistors with a dual-gate structure can make full use of the dual surface conductive channels of 2D-TMDCs to achieve different logic functions (Figure 2B): unipolar p- or n-type materials can realize linear logic functions, such as OR and AND, and forming a logic unit with bipolar materials can realize nonlinear logic functions, such as XNOR [22]. As shown in Figure 2C, compared with the carbon nanotube and NMOS circuits, the number of transistors consumed by the XNOR, NOR, and OR logic gates formed by the double-gate transistor is reduced from 10,

4, and 2, respectively, to one transistor, which can effectively reduce the circuit complexity [23–25].

Logic function changes can also be adjusted by the thickness of the 2D material, ultimately building PCC FETs (Figure 2D) [16]. When the thickness of MoS<sub>2</sub> is less than 4 nm, the thickness of the channel is less than the shield length of the material, and a negative voltage is an input to either gate, leaving the transistor in the off state, thus achieving AND logic functionality. When thick MoS<sub>2</sub> is used as the channel material, the top and bottom gates without influencing each other, and OR logic functions can be achieved. In the meantime, light illumination can significantly increase the number of carriers in the channel material. In the few-layer MoS<sub>2</sub> transistor, coupling light illumination to the logic device enables optical switching between OR and AND logic functions. Therefore, one transistor can achieve the logic functions that require two devices in conventional Si CMOS, greatly improving the computing capability of transistors.

The basic logic functions are realized by using the material intrinsic properties, and further complex logic functions can be constructed by interconnection. Among them, the half-adder is the basic device in the combinational circuit and the center of the processing operation in the logic circuits [26,27]. In Figure 2E, a WSe<sub>2</sub> transistor, MoS<sub>2</sub> transistor, and two resistors (2T2R) are connected to realize the one-bit half-adder function. As shown in Figure 2F, this half-adder has a precise logic function. In conventional CMOS logic circuits, more than ten transistors are required to construct a half-adder, while the use of 2T2R circuits reduces this number to two, saving transistor count while achieving the same logic function [28,29]. In addition, multi-functional devices, which are available as high-performance diodes, transistors, photo-detectors, and programmable rectifiers, can be constructed by van der Waals integration of 2D materials, without the need to consider lattice matching [12].

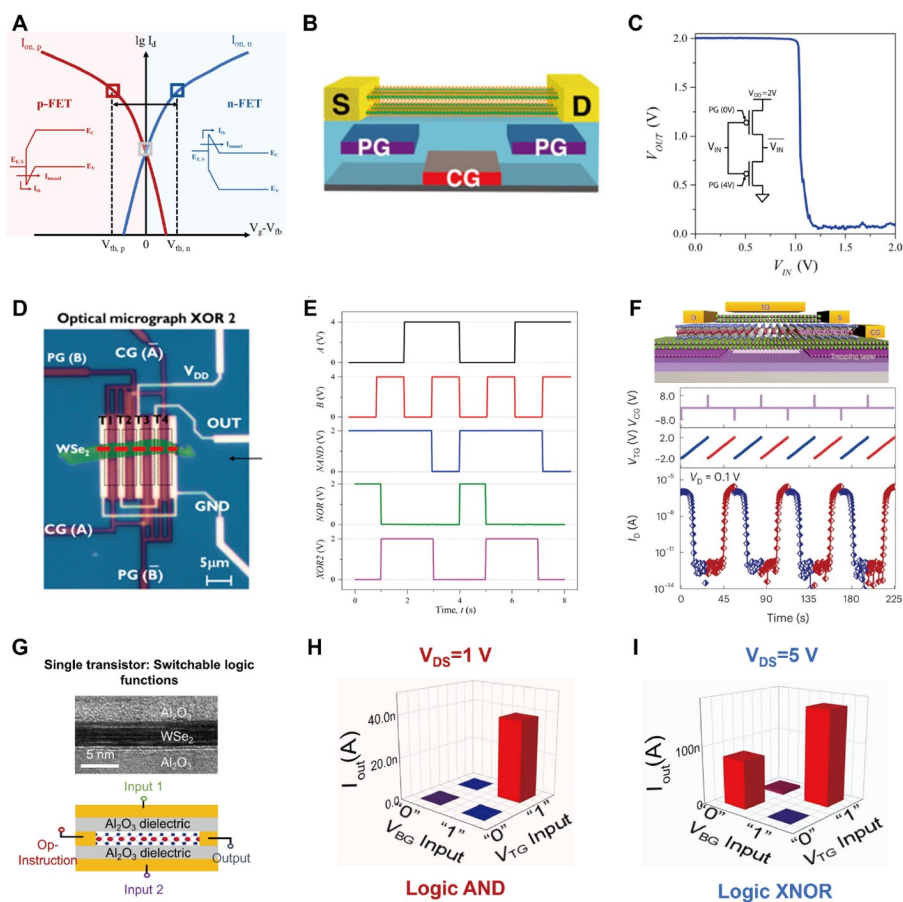
The intrinsically diverse material system, atomic layer structure, and excellent double interface gate control properties of 2D-TMDCs show great potential in the realization of PCC transistors. By varying the intrinsic properties such as material polarity and thickness, the computing-capability limits of conventional transistor architectures are broken. Simultaneously, multiple complex logic functions are accomplished using a single transistor, significantly improving the computing capability of transistors and reducing the number of transistors. A small number of novel PCP transistors achieve complex logic functions, and optimize circuit complexity. However, the switching of logic functions relies on different channel materials, and the problem of cumbersome selection of material polarity and its thickness is not favorable to large-scale integration, posing a challenge to apply it to logic circuits.

### **Device structure design for 2D-TMDCs-based PCC logic circuits**

Compared with conventional Si-based materials, 2D materials have excellent bipolar electrical properties at the atomic layer thickness, making it easier to use gates to modulate their transport properties and thus realize different logic functions [30,31]. The most direct way of gate modulation is the electrostatic gate voltage applied to the dielectric layer, and the resulting field can modulate the Fermi level of the 2D materials located on the dielectric layer [12,32]. Using the bipolar WSe<sub>2</sub> as the channel, the bottom gate regulates its Schottky barrier height to achieve a shift in material polarity, while the top gate can be used as the logic input to construct a PCC FET [33]. Ideally, when the bottom gate voltage is positive, electron transport can be achieved at a positive top gate voltage. Because the Fermi level of the electrode is close to the conduction

band minimum of WSe<sub>2</sub>, which has a small barrier at the conduction band, and a high hole barrier with the valence band, which suppresses hole transport. As a result, the device exhibits the n-type behavior (blue line in Figure 3A). Conversely, at a negative bottom gate voltage, the device exhibits a p-type carrier-dominated behavior (red line in Figure 3A). When the bottom gate voltage is zero, the Fermi level at the bottom is close to the bandgap middle of WSe<sub>2</sub>, and the electron barrier height and hole barrier height are similar. So the device can achieve n-type electron transport at positive top gate voltage and p-type hole transport at negative top gate voltage, and thus the device exhibits bipolar transport characteristics [34].

From the design of the device structure (Figure 3B), multiple bottom gates are used to regulate the channel and contact region respectively: programmed gate (PG) and control gate (CG). When the CG gate voltage is less than 0 V, the holes can be injected into the channel, and the WSe<sub>2</sub> transistor is modulated as a p-type



**Figure 3** Device engineering for 2D-TMDCs-based PCC logic devices. (A) Output characteristic curves of 2D FETs under different polarities. Inset is the schematic band diagram when the semiconductor is in contact with metal. Red represents p-type carrier transport; blue represents n-type carrier transport. (B) Schematic diagram of the WSe<sub>2</sub> transistor based on control gate modulation. (C) CMOS inverter via polarity-controlled gates. Inset: circuit schematic of the inverter. (D) Optical microscope imaging of four transistors forming a logic circuit. (E) Polarity-controllable WSe<sub>2</sub> FETs implemented by NAND, NOR, and XOR output waveforms. (B)–(E) Reproduced with permission from [36]. Copyright©2018, American Chemical Society. (F) Schematic diagram of polarity-controlled WSe<sub>2</sub> FETs based on floating gate structure and different polarities by pulse voltage. Reproduced with permission from [38]. Copyright©2022, Springer Nature. (G) Top: cross-sectional high-resolution transmission electron microscopy image. Bottom: schematic diagram of the dual-gate WSe<sub>2</sub> FETs structure. The drain and source of the device are used as OP command and output ports, and the vertical dual-gate gates are used as logic inputs. With the OP command signal input, a single transistor can perform switchable logic functions. (H) Dual-gate WSe<sub>2</sub> FET for AND logic at a low operating voltage ( $V_{DS}=1$  V). (I) Dual-gate WSe<sub>2</sub> FETs for XNOR logic at high operating voltage ( $V_{DS}=5$  V). (G)–(I) Reproduced with permission from [40]. Copyright©2022, Springer Nature.

transistor. In contrast, the WSe<sub>2</sub> transistor is regulated to an n-type transistor when the gate voltage of the CG is 3 V. The on/off ratios of n-type and p-type transistors achieved with polar gate modulation of carrier transport are 10<sup>5</sup> and 10<sup>6</sup>, respectively. Complementary inverters were successfully constructed based on the control gate modulation in Figure 3C.

The polarity of the material is generally regulated by PG, and CG is used as the logic input. Based on conventional CMOS circuits, NAND and NOR logic functions can be realized, but it increases the complexity of device construction and is not conducive to integrated design [35]. The advantage of using PG-controlled carrier transport types is that using PG as a logic input greatly increases the flexibility of device design and significantly improves the computing capability of transistors [36]. As shown in Figure 3D, the highly compact connection of four polarity-controlled transistors, with logic input A applied to CG and logic input B applied to PG, ultimately enables the logic functions XOR and MAJ. Compared with conventional CMOS circuits, this transistor significantly reduces the number of transistors. By replacing the  $V_{DD}$  and GND terminals, the three-input logic functions XOR-3 and MAJ-3 can be realized using four transistors (Figure 3E). XOR-3 and MAJ-3 are basic logic functions in logic circuits, but in CMOS logic circuits, the implementation of this logic function generally requires the interconnection of dozens of transistors to form a logic cell, thus having a complex logic circuit. Therefore, the use of polarity-controlled transistors can significantly improve the computing-capability of transistors and reduce circuit complexity.

The electrostatic gate voltage regulation is immediate as a direct regulation means, and when the voltage of CG is removed, the polarity regulation effect disappears at the same time, so it is not suitable for low-power operation. The effective integration of memory devices with logic devices, where the material polarity is regulated by a floating gate and the basic logic functions are realized, shows great potential for high-density integration [27,37]. Among them, the PG is replaced with a graphene floating-gate storage structure, and the top gate is used as CG. The polarity of WSe<sub>2</sub> can be effectively regulated by pulse voltage (Figure 3F), and the floating-gate layer has a strong charge capture and storage capability for a charge, which gives the device good non-volatile retention characteristics [38]. Using different channel materials, the circuit can realize XOR and AND logic functions. Moreover, the successful implementation of a half adder using only one WSe<sub>2</sub> transistor and one MoS<sub>2</sub> transistor provides a new idea for the design of non-volatile PCC transistors.

Currently, to solve the circuit redundancy problem in parallel computing and improve the computing capability of the transistor, compact transistor architectures with multiple logic functions switchable need to be designed. The key point at the core of using a gate to regulate the transport characteristics of transistors is to regulate the Schottky barrier in the contact region, and the main carriers in the channel material WSe<sub>2</sub> gradually change from electrons only to electrons and holes by using different bias voltages  $V_{DS}$ , as shown in Figure 3G [39,40]. Therefore, with a vertical double gate as the logic input, a switchable logic function can be achieved by changing the bias voltage without an additional control terminal. When the  $V_{DS}$  is 1 V, the hole-dominated output current is much smaller than the electron-dominated output current, and the corresponding transistor exhibits a logic function AND in Figure 3H. When the  $V_{DS}$  is 5 V, the hole current is almost the same as the electron current, and the XNOR logic function can be realized using the vertical dual gate (Figure 3I). Compared with CMOS complex logic circuits, this compact WSe<sub>2</sub> transistor can switch between AND and XNOR logic functions without the need for complex multiplexer circuits and can realize multiple functions with a single transistor, greatly reducing circuit redundancy and improving the computing-capability of transistors.

## Architecture design of 2D-TMDCs-based PCC logic circuits

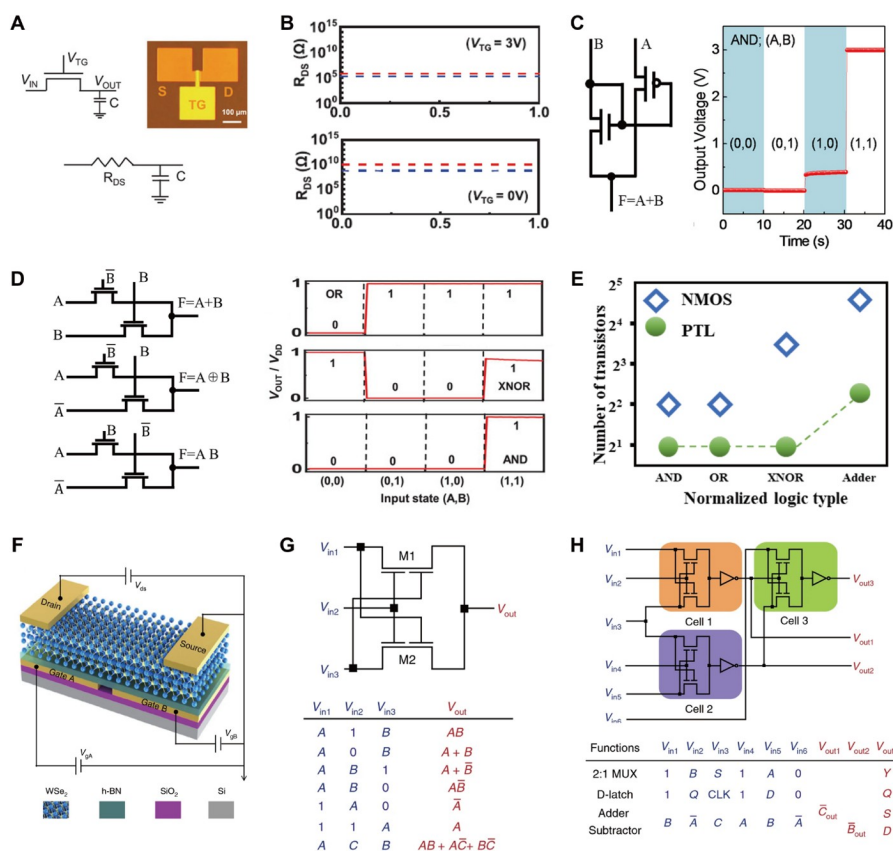
Static CMOS logic circuits are based on inverters that are extended to have multiple inputs and thus achieve combinational logic functions. Similar to inverters, static CMOS logic circuits have good stability and low static power consumption. However, the circuit design has a significant redundancy problem, requiring at least  $2N$  transistor interconnections to perform operations on  $N$  input signals. Therefore, an excessive number of transistors is required in the logic circuit, which is not conducive to the realization of designing high-density logic circuits. In addition, the grown TMDCs usually exhibit n-type transport characteristics due to material quality issues, such as the presence of chalcogenide vacancies [41]. This leads to the fact that most of the demonstrated logic circuits are based on pseudo-NMOS structures, which severely limits the development of PCC transistors while increasing power consumption compared to CMOS logic circuits [24,42]. Therefore, it is critical to design suitable circuit architectures for 2D material customization.

Pass transistor logic (PTL) configuration is a widely used alternative in logic circuits that can improve the computing capability of transistors [43]. In static CMOS logic circuits or pseudo-NMOS circuits, the signal is input from the gate of the FET only, with the source and drain acting as supply. Therefore, logic functions can only be increased by increasing the number of FETs. In PTL circuits, the signal can be input from the gate of the FET, or from the source or drain (Figure 4A), and two transistors are sufficient for the basic logic function, which significantly reduces the number of transistors [44]. In the n-type MoS<sub>2</sub>-FET, when the top gate voltage is 3 V, the MoS<sub>2</sub> channel resistance  $R_{DS}$  is about  $10^5 \Omega$ . At this time, the FET is in a “low resistance” state (Figure 4B), so the input signal  $V_{IN}$  can be transmitted from the source to the drain. When the gate voltage is 0 V,  $R_{DS}$  is greater than  $10^8 \Omega$ . At this point, the FET is in a “high resistance” state, so the input signal  $V_{IN}$  cannot be transmitted to the output. Based on PTL circuits, CMOS FETs fabricated with n-MoS<sub>2</sub> and p-WSe<sub>2</sub> successfully demonstrate logic functions: NOT, AND (Figure 4C), OR [45]. However, at high gate voltages, the non-zero output resistance weakens the high-level output and there is a voltage loss. For this reason, a signal loss can be repaired by cascading inverters to achieve a high-precision logic function.

With the PTL circuit, two MoS<sub>2</sub>-FETs connected in series can realize the basic logic functions: AND, OR, and XNOR, and exhibit accurate logic functions in Figure 4D [46]. In contrast, in CMOS combinational logic circuits, the number of transistors required to realize these three logic functions is 4, 4, and 10, respectively (Figure 4E). In addition, the full adder is a core unit widely used in logic circuits. In CMOS circuits, 28 FETs are required to realize the 1-bit full adder function, while using the PTL structure, 6 transistors can construct a full adder, significantly improving the computing capability of transistors and simplifying the logic circuits. While reducing the number of transistors consumed, PTL circuits have the potential to increase the speed of logic operations and reduce operating power consumption.

The 2D material exhibits various transport characteristics at different gate voltages, which greatly facilitates the design of complex logic functions using PTL circuits. As shown in Figure 4F, electrically tunable homojunction (ETH) is constructed with the bipolar material WSe<sub>2</sub> [47]. The homojunction transport characteristics of the device can be dynamically regulated by the voltage magnitude of gate A and gate B. With the PTL structure, two ETHs are connected in series to form a logic cell to realize the basic logic functions. Seven logic functions are realized when different logic inputs are configured in Figure 4G. Further, by cascading logic cells and configuring different logic values at the input ports, 2:1 multiplexer, D-locker, and 1-bit full adder and subtractor logic functions can be implemented in the same device (Figure 4H). The





**Figure 4** Circuit architecture design engineering for 2D-TMDCs-based PCC logic device. (A) Schematic diagram of a single transistor with PTL circuit architectures, with the gate used to moderate the channel resistance  $R_{DS}$  and the input signal  $V_{IN}$  able to transfer from the source to the drain. (B) Different  $R_{DS}$  when the FET is in the on-state and off-state. The red curve means transfer logic “1” and the blue curve means transfer logic “0”. (C) AND logic circuit of a PTL circuit based on n-MoS<sub>2</sub> with p-WSe<sub>2</sub> CMOS. Reproduced with permission from [45]. Copyright©2015, American Chemical Society. (D) Circuit diagrams and output waveforms for different logic functions (AND, OR, XNOR). (A), (B), (D) Reproduced with permission from [46]. Copyright©2022, John Wiley and Sons. (E) Comparison of the number of transistors consumed by PTL architecture and pseudo-NMOS to implement different logic functions. (F) Schematic diagram of the ETH device. (G) Seven logic functions implemented based on two ETH devices configured with different logic inputs. (H) Logic single-cell cascade implementing multiplexer, D-latch, 1-full adder, and subtractor logic functions. (F)–(H) Reproduced with permission from [47]. Copyright©2020, Springer Nature.

use of ETH to implement logic functions not only reduces the complexity of the fabrication process but also reduces the number of transistors, thus offering promise in simplifying logic circuits.

### Challenges for future developments of 2D-TMDCs-based PCC logic circuits

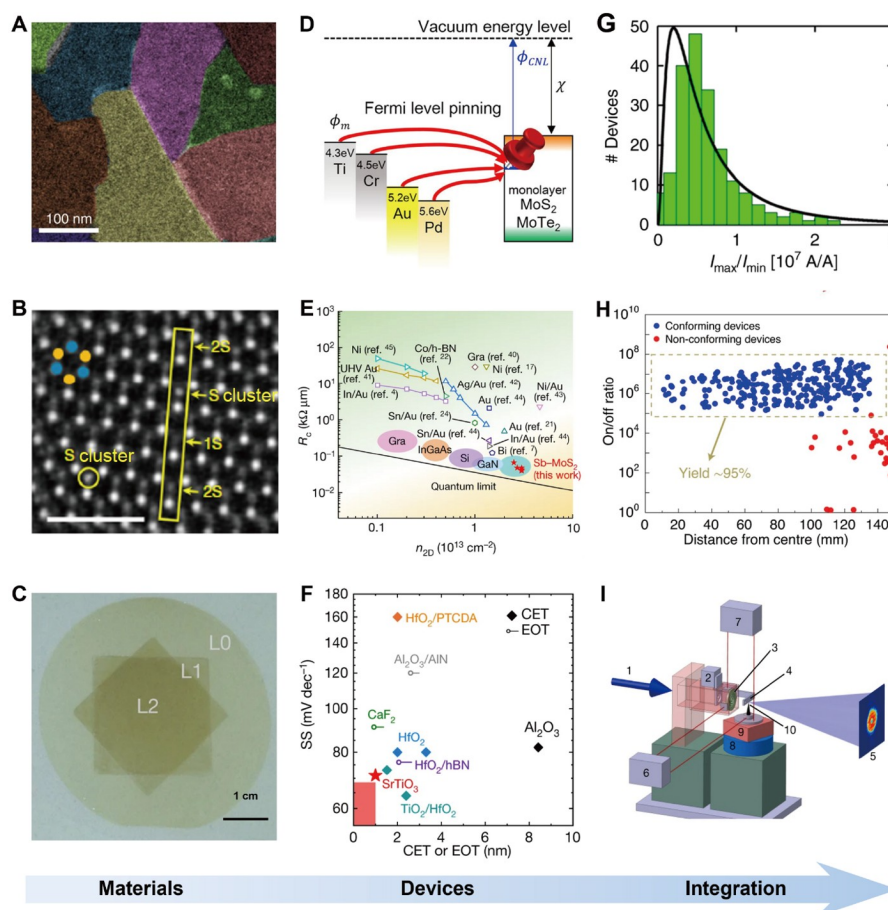
A large number of prototype devices demonstrate the great potential of 2D-TMDCs-based PCC FETs for future logic circuit applications (Table 1). However, 2D-TMDCs-based PCC FETs development is still in its infancy. From the laboratory to industrial semiconductor applications, in-depth research is required in materials, device construction, and integration.

High-quality fabrication of wafer-level 2D-TMDCs is the foundation of logic circuit applications. Currently, 2D-TMDCs PCC transistors are mainly constructed using mechanically exfoliated materials, which

**Table 1** Comparison of transistor consumption of various logic devices

Device	Logic function	Transistor number	Ref.
Traditional transistor architectures (CMOS)	XNOR	12	
	AND	6	–
	OR	6	
Traditional transistor architectures (NMOS)	XNOR	10	
	AND	4	–
	OR	4	
Polarity-controlled types of transistors	XNOR	1	
	NOR	1	[22]
Thickness control type transistors	OR	1	
	OR&AND	2	[16]
WSe <sub>2</sub> transistor with multiple bottom gates	XOR&AND&NOR	4	[36]
Transistors of the floating gate regulation type	NAND&NOR	2	[38]
	XOR&XNOR	1	
LNO-based WSe <sub>2</sub> transistor	AND	2	
	OR	2	[48]
Compact WSe <sub>2</sub> transistor	NAND&NOR	2	[40]
MoS <sub>2</sub> pass-transistor logic circuit	XNOR&AND&OR	2	[46]
WSe <sub>2</sub> electrically tunable homojunction	AND&OR	2	[47]

are inefficient and difficult to apply to large-scale circuits. Many large-area deposition methods for 2D-TMDCs have been developed [49–53]. Chemical vapor deposition (CVD) is a simple and controllable, industry-compatible, low-cost method that promises the industrialization of wafer-scale 2D-TMDCs through growth process optimization [54]. During the material growth process, a large number of nucleation points are formed randomly on the substrate surface, and when the nucleation points gradually grow and splice with each other, a large number of grain boundaries will be formed (Figure 5A) [55,56]. Furthermore, regardless of the preparation method used, there are always defects in the material and it is almost impossible to produce a perfect structure [57]. As shown in Figure 5B, similar to conventional materials, the defects in 2D TMDCs are mainly point defects and line defects [58,59]. Such defects and grain boundaries can be the electron scattering centers, leading to enhanced carrier scattering and seriously deteriorating the performance of TMDCs devices [60,61]. In particular, as carrier scattering increases, its mobility and on-state current are also affected and reduced, which is not beneficial to low-power consumption and high-speed operation [62]. The presence of defects can also lead to defect binding states in the band gap of TMDCs materials. The presence of such defect states, especially deep energy level defect states, can lead to the Fermi level pinning of the material, leaving the polarity of the material unregulated by the gate [63]. This is deadly damage to the development of PCC transistors. At the same time, when the material has defects, it will be more likely to attract molecules such as water and oxygen from the air, further damaging the material [64]. In addition, most of the materials prepared are n-type materials and few high-quality p-type and bipolar materials are available, which limits the development of PCC transistors for large-scale integration. As interfacial charge impurities and inherent structural defects not only hinder the high-performance operation of the device but also lead to strong electron doping of the material, which results in most 2D materials exhibiting an n-type transport type. The Fermi level pinning at the metal/2D semiconductor interface leads to a large Schottky barrier height for hole injection, which also greatly hinders p-type conduction in 2D materials [65]. For typical bipolar materials such as WSe<sub>2</sub> and MoTe<sub>2</sub>, not only is it difficult to balance p- and n-type transport, but their



**Figure 5** Challenges for future development of 2D-TMDCs-based logic circuits. (A) Pseudo-color dark field transmission electron microscopy image of MoS<sub>2</sub>. Reproduced with permission from [56]. Copyright©2019, Springer Nature. (B) High-angle annular dark field image of MoS<sub>2</sub> clearly shows different sulfur vacancy types. Reproduced with permission from [59]. Copyright©2017, Springer Nature. (C) Multilayer 2D MoS<sub>2</sub> films obtained by layer-by-layer transfer. Reproduced with permission from [71]. Copyright©2017, Springer Nature. (D) Schematic diagram of Fermi pinning formed by metal and 2D MoS<sub>2</sub>. Reproduced with permission from [65]. Copyright©2017, American Chemical Society. (E) Contact resistance versus carrier density of 2D MoS<sub>2</sub> transistors, with semi-metallic Sb achieving ultra-low contact resistance. Reproduced with permission from [81]. Copyright©2022, Springer Nature. (F) EOT versus subthreshold slope (SS) for different dielectric layers. Reproduced with permission from [89]. Copyright©2022, Springer Nature. (G) Switching ratio variation of several hundred MoS<sub>2</sub> transistors. Reproduced with permission from [90]. Copyright©2020, Springer Nature. (H) Yield of integrated WS<sub>2</sub> transistors. Reproduced with permission from [93]. Copyright©2022, Springer Nature. (I) Diagram of a high-resolution non-destructive 3D imaging device. Reproduced with permission from [96]. Copyright©2017, Springer Nature.

chemical reaction energies are large and the preparation conditions are demanding. And the relatively small variety of bipolar materials severely limits their wide application. Therefore, there is an urgent need to develop high-quality wafer-level 2D single-crystal TMDCs preparation methods to lay the material foundation for the development of 2D-TMDCs PCC transistors.

High-quality material preparation usually requires high temperatures, which is not compatible with current Si-CMOS technology [66]. Therefore, the CVD-grown 2D-TMDCs need to be transferred to the target substrate, which may severely damage the material properties. Currently, impurity residues and non-destructive transfer of wafer-level materials remain a challenge for the transfer process. Most 2D-TMDCs transfer methods require organic assistance and some require immersion with chemical solutions

(Figure 5C), which leads to the presence of organic residues on the material surface, further affecting the electron transport properties of 2D-TMDCs, as shown in Figure 5C [67–71]. In addition, the nondestructive transfer technology for large-area TMDCs is still in the early stage of research and fails to meet the requirements of practical device applications. Therefore, the development of nondestructive transfer techniques for wafer-level 2D-TMDCs is crucial for device applications.

As the device size continues to miniaturize, the metal and dielectric layers deposited on the 2D-TMDCs are a major limitation to increasing the computing capability of transistors. During vapor deposition of metal, high-energy metal atoms destroy the 2D-TMDCs atomic lattice generating defects that result in the Fermi level being pinned by the interfacial state (Figure 5D), and the potential barrier height is independent of the metal work function [65,72]. For 2D-TMDCs-based PCC FETs applications, the core of tuning the FETs transport characteristics is to modulate the 2D semiconductor-metal contact barrier by the gate voltage. When the Fermi level pinning effect is present at the interface, especially for bipolar materials such as  $\text{WSe}_2$ , the device can only exhibit a single transport characteristic and is unable to modulate its polarity through the gate, limiting the functionality of extended individual transistors [73]. Fermi pinning leads to high contact resistance between the metal and the 2D material, which limits the maximum on-state current of the transistor and further hinders the device's operation speed [74]. The development of van der Waals contacts is an effective method to reduce contact resistance [75–78]. The use of low-melting point semimetals in contact with 2D-TMDCs suppresses the metal-induced gap state and avoids the generation of Fermi pinning, which in turn greatly reduces the contact resistance [79,80]. A good ohmic contact is formed between the semimetal antimony (Sb) and  $\text{MoS}_2$ , which fully suppresses the metal-induced state and achieves the lowest contact resistance. This contact resistance is close to the quantum limit and is comparable to advanced three-dimensional semiconductors, as shown in Figure 5E [81]. However, few p-type 2D materials have low resistance contacts with metals [82]. Therefore, there is an urgent need to establish high-quality van der Waals contact methods compatible with Si CMOS processes to promote the development of 2D-TMDCs-based PCC devices.

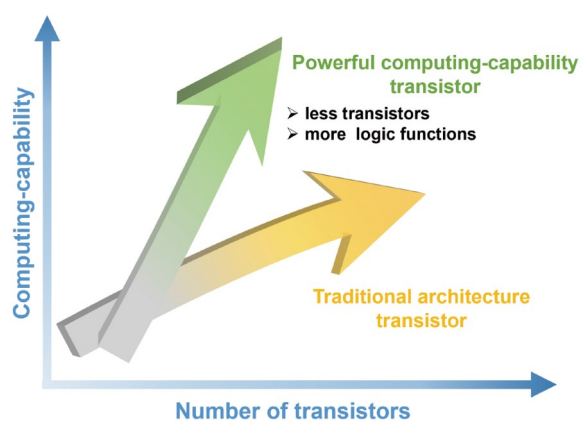
In most PCC transistors, it is challenging to produce dielectric layers with the same properties on the top and bottom surfaces of the 2D-TMDCs, especially when high-quality, ultra-thin dielectric layers are required on top of 2D-TMDCs [83]. The advantage of having no dangling bonds on the surface of the 2D-TMDCs becomes a disadvantage. The smooth surface makes it difficult to provide nucleation sites for the deposition of dielectric layers, and the low quality of the dielectric layer formed on its surface makes it difficult to control device performance using top gates [84]. Its bottom gate alone acts similarly to the top gate effect of a conventional Si base, but that is not suitable for application in PCC transistors. Although various interfacial passivation processes have been developed, defects and severe doping effects, especially n-type doping, have been generated in the channel material [85,86]. Even the majority of PCC transistors constructed with bipolar  $\text{WSe}_2$  exhibit n-type transport characteristics, making it difficult to regulate their polarity even at the gate, which severely limits the use of 2D-TMDCs in PCC transistors. The development of high-performance van der Waals dielectric layers offers a promising strategy for creating high-performance electronic devices. Liao *et al.* [83] reported a unique ozone treatment of  $\text{HfS}_2$  flakes to transform into  $\text{HfO}_x$  to widen the  $\text{MoS}_2$  and  $\text{HfO}_x$  van der Waals gap and suppress dielectric defects and channel material interactions, enabling the construction of the high-performance  $\text{MoS}_2$  transistors and logic circuits. Besides, high dielectric constant single crystal perovskite strontium titanium oxide ( $\text{SrTiO}_3$ ) films are an excellent dielectric layer material

[87,88]. The SrTiO<sub>3</sub> dielectric layer is constructed by transfer technique, forming a van der Waals interface with the 2D-TMDCs and maintaining the intrinsic properties of the 2D material (Figure 5F) [89]. However, the narrow band gap of SrTiO<sub>3</sub> greatly reduces the advantages of its application in FETs. Therefore, in-depth studies in the wide bandgap, van der Waals dielectric layers with equivalent oxide thickness (EOT) = 1 nm are still required.

In terms of device integration, researches on developing logic circuits with PCC transistors stop at specific devices, and more complex, large-scale logic circuits remain in a gap. From individual devices to large-scale circuit applications, device differences, and yield are major challenges in developing transistor integration [90–93]. The logic circuits preparation process is inevitably damaging to the material, especially the introduction of defects, which can cause a variation in device performance. When the influence of the introduced defects is too great, even though the device performs well, the large device-to-device variation can lead to circuit disorder and failure to operate the logic, which can significantly reduce the yield. To improve the yield of the devices, further efforts are needed to optimize the fabrication process and avoid material damage. On the other hand, the scaling down of transistors to the nanometer level and the formation of complex three-dimensional structures due to vertical stacking make it difficult to properly evaluate logic circuits' performance [94,95]. As shown in Fig. 5I, X-ray is a powerful technique for efficient non-destructive testing of logic circuits due to their strong penetrating properties and high resolution [96]. In addition, in the future, improving circuit robustness is critical [42,97].

## Outlook

In summary, 2D-TMDCs-based PCC FETs utilize the unique properties of ultrathin 2D materials to the utmost and provide a revolutionary solution for developing efficient computations. Currently, 2D-TMDCs-based transistors have demonstrated the advantages of optimized circuit complexity and efficient computation in simple logic devices. To make the transition from laboratory to industrial applications, there are still some challenges to be solved. (1) High-quality wafer-scale 2D single crystal TMDCs preparation, including controlled growth and lossless transfer. (2) Fabrication of high-performance FETs with low contact resistance and low EOT. (3) Establishment of circuit integration methods compatible with silicon technology and their standardized processes and test systems. Once breakthroughs are made in materials, devices, and circuit integration, 2D-TMDCs-based PCC FETs will be one of the key paths for the development of post-silicon logic circuits. Faced with the growing demand for computing capability, 2D-TMDCs-based transistors can be developed in two different technology routes to continue to drive the advancement of PCC logic circuits (Figure 6). One is the application of 2D materials into conventional architecture transistors; the other is the use of 2D TMDCs to fabricate new-principle PCC transistors. One of the first possibilities is to build 2D-TMDCs-based logic circuits by traditional architectures, to relieve the arithmetic demand to some extent. As the 2D-TMDCs-based PCC transistors are further developed and applied to logic circuits, this will exceed the computing capability of logic circuits based on traditional transistor architectures. Unlike traditional architectures, PCC transistors can save the number of transistors consumed in logic circuits for the same computing requirements. The development of 2D-TMDCs-based PCC transistors may need to overcome more difficult challenges than traditional architecture transistors, including brand-new device simulation and



**Figure 6** Two different development routes of 2D-TMDCs-based transistors for future logic circuits.

circuit system architecture design. Still, we believe that only by designing 2D-TMDCs-based PCC transistors based on the original circuit space and integrating more logic functions, can we break through the computing-capability improvement bottleneck of silicon-based logic circuits.

### Data availability

The original data are available from corresponding authors upon reasonable request.

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### Author contributions

X.Z., H.Z., X.W., Y.Z., Z.Z., and Yue Zhang contributed to the discussions and revised the manuscript. Yue Zhang and Z.Z. supervised the project. All authors have read and improved the manuscript.

### Conflict of interest

The authors declare no conflict of interest.

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